



Si2333DDS

P-Channel 12 V (D-S) MOSFET

MOSFET PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^a	Q _g (Typ.)
- 12	0.028 at V _{GS} = - 4.5 V	- 6 ^e	9 nC
	0.032 at V _{GS} = - 3.7 V	- 6 ^e	
	0.040 at V _{GS} = - 2.5 V	- 6 ^e	
	0.063 at V _{GS} = - 1.8 V	- 4.5	
	0.150 at V _{GS} = - 1.5 V	- 3.6	

FEATURES

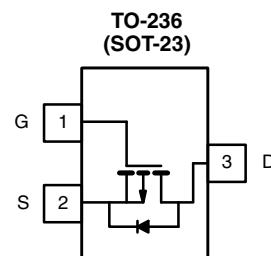
- TrenchFET® Power MOSFET
- 100 % R_g Tested



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Smart Phones and Tablet PCs
 - Load Switch
 - Battery Switch



Top View

Si2333DDS (O4)*

* Marking Code

Ordering Information: Si2333DDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 12	V	
Gate-Source Voltage	V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	- 6 ^e	A
	T _C = 70 °C		- 5.2	
	T _A = 25 °C		- 5 ^{b, c}	
	T _A = 70 °C		- 4 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 20	W	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 1.4	
	T _A = 25 °C		- 0.63 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	1.7	
	T _C = 70 °C		1.1	
	T _A = 25 °C		1.20 ^{b, c}	
	T _A = 70 °C		0.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	100	130	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	60	75	

Notes:

- a. Based on T_C = 25 °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 175 °C/W.
- e. Package limited.

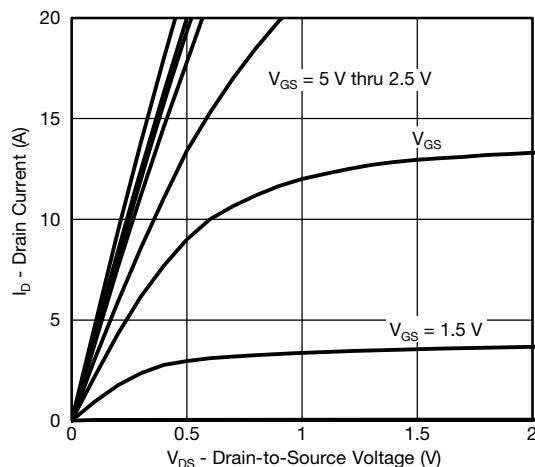
**MOSFET SPECIFICATIONS** ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$		-8		$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			2.4		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$		0.023	0.028	Ω
		$V_{GS} = -3.7 \text{ V}, I_D = -4.6 \text{ A}$		0.026	0.032	
		$V_{GS} = -2.5 \text{ V}, I_D = -4.3 \text{ A}$		0.033	0.040	
		$V_{GS} = -1.8 \text{ V}, I_D = -1 \text{ A}$		0.048	0.063	
		$V_{GS} = -1.5 \text{ V}, I_D = -0.5 \text{ A}$		0.075	0.150	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5 \text{ V}, I_D = -5 \text{ A}$		18		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -6 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1275		pF
Output Capacitance	C_{oss}			255		
Reverse Transfer Capacitance	C_{rss}			236		
Total Gate Charge	Q_g	$V_{DS} = -6 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -5 \text{ A}$		23	35	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -6 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$		14	21	
Gate-Drain Charge	Q_{gd}			2.3		
Gate Resistance	R_g			3.6		
Turn-On Delay Time	$t_{d(\text{on})}$	$f = 1 \text{ MHz}$ $V_{DD} = -6 \text{ V}, R_L = 6 \Omega$ $I_D = -4 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 1 \Omega$	1.9	9.5	19	Ω
Rise Time	t_r			26	40	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			24	40	
Fall Time	t_f			45	70	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			-1.4	A
Pulse Diode Forward Current ^a	I_{SM}				-20	
Body Diode Voltage	V_{SD}	$I_S = -4 \text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -4 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		24	48	ns
Body Diode Reverse Recovery Charge	Q_{rr}			8	16	nC
Reverse Recovery Fall Time	t_a			9		
Reverse Recovery Rise Time	t_b			15		

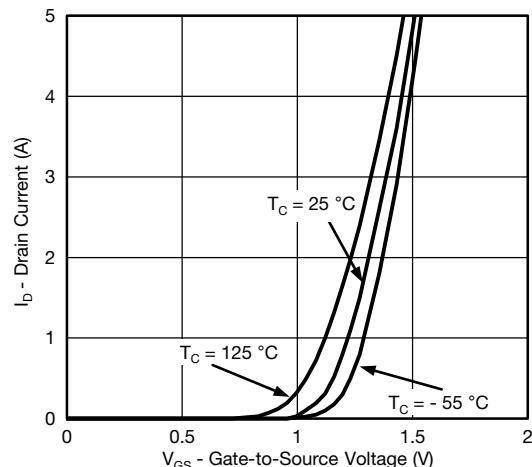
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

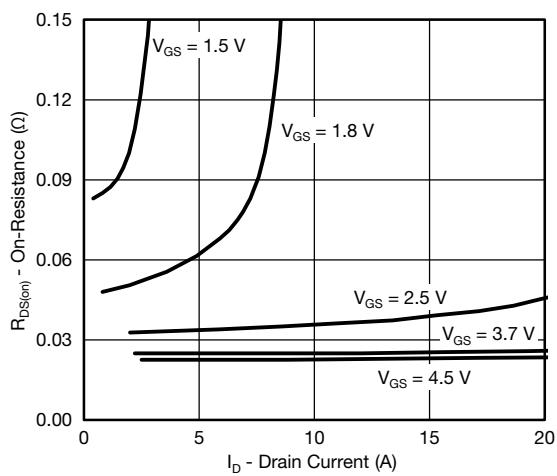
b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

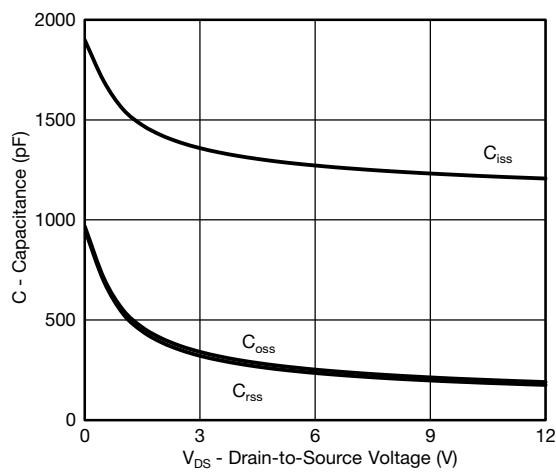
Output Characteristics



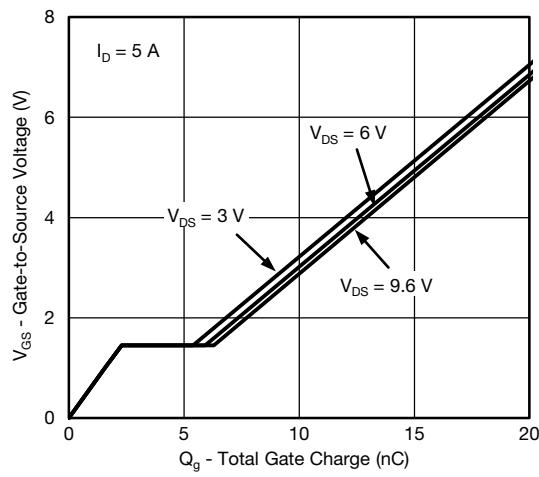
Transfer Characteristics



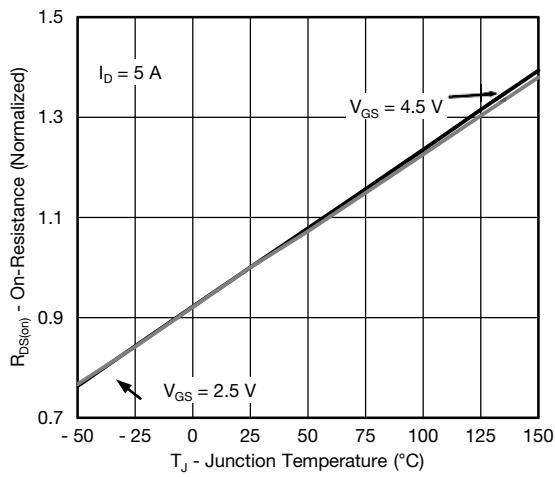
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



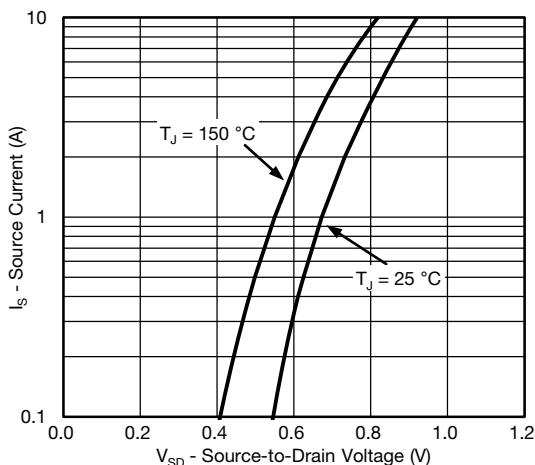
Gate Charge



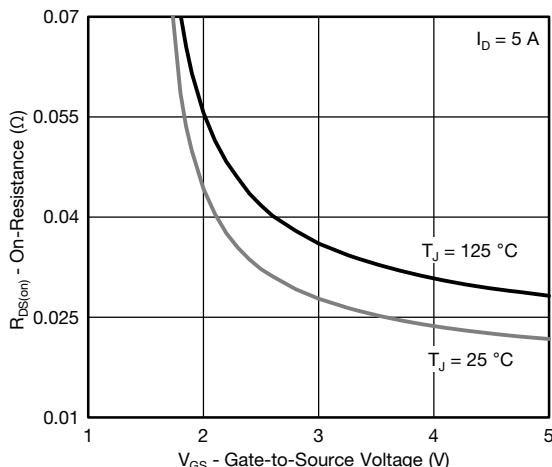
On-Resistance vs. Junction Temperature



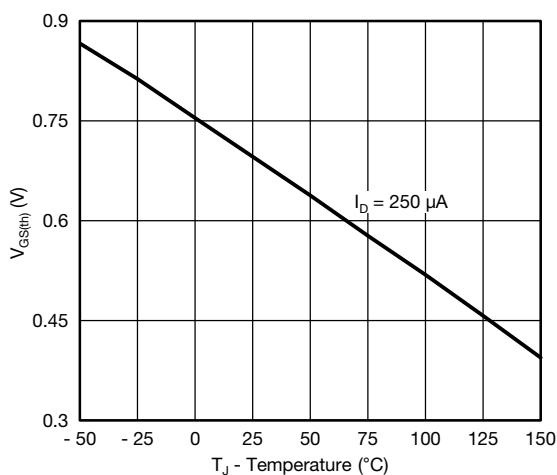
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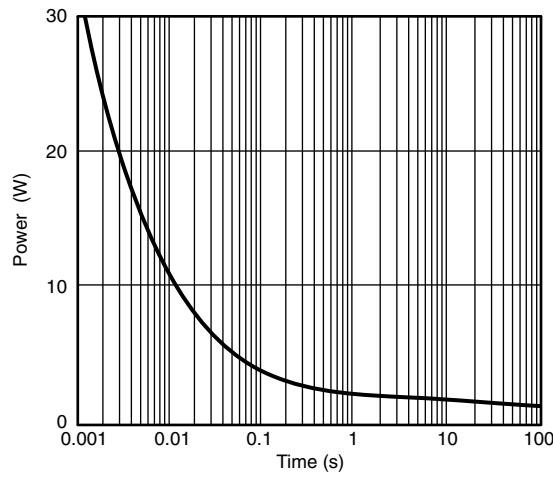
Source-Drain Diode Forward Voltage



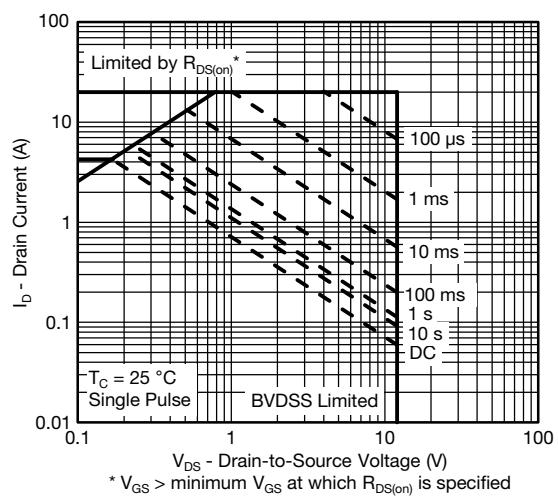
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



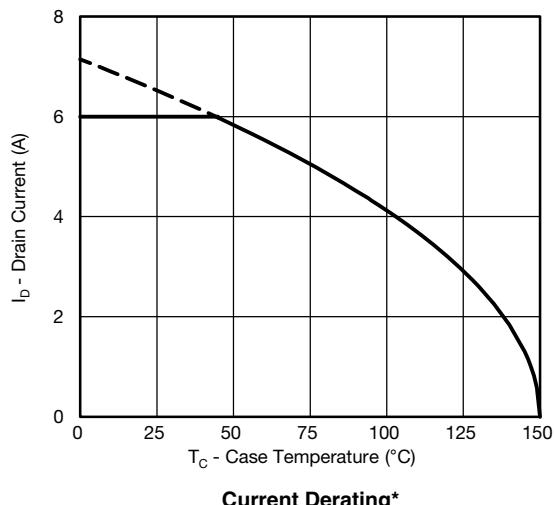
Single Pulse Power



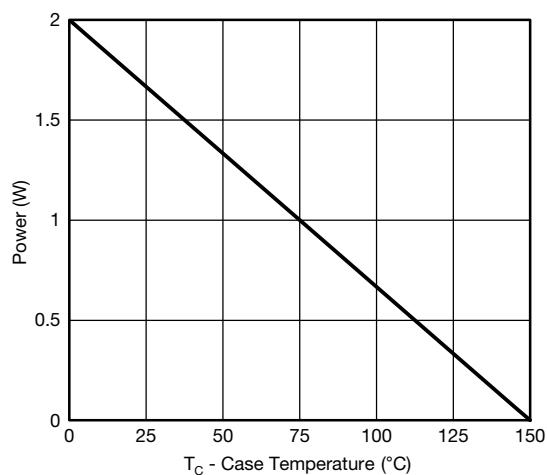
Safe Operating Area



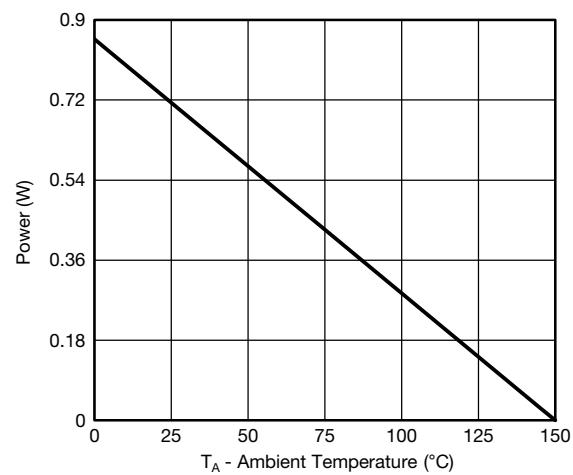
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

