



N-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The 4410A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

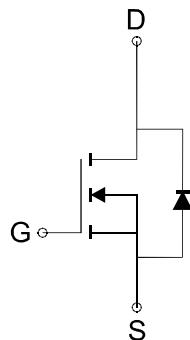
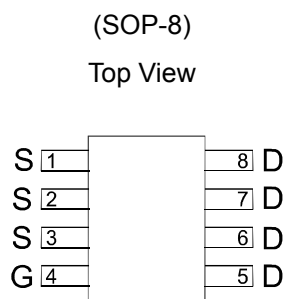
FEATURES

- $R_{DS(ON)} \leq 12m\Omega @ V_{GS}=10V$ (Typ)
- $R_{DS(ON)} \leq 17m\Omega @ V_{GS}=4.5V$ (Typ)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

PIN CONFIGURATION



N-Channel MOSFET

e Ordering Information: 4410A (Pb-free)

4410A-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

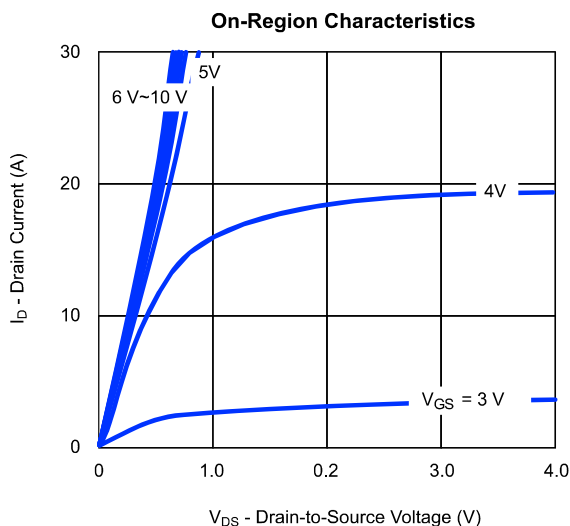
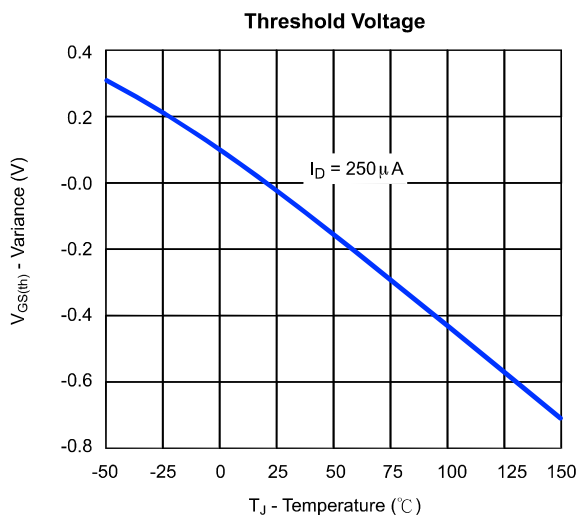
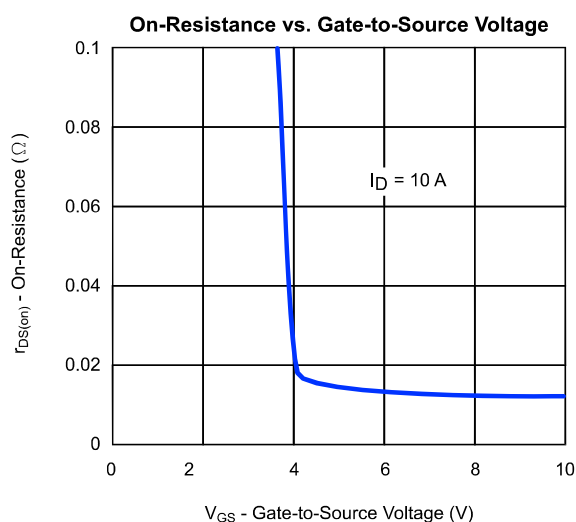
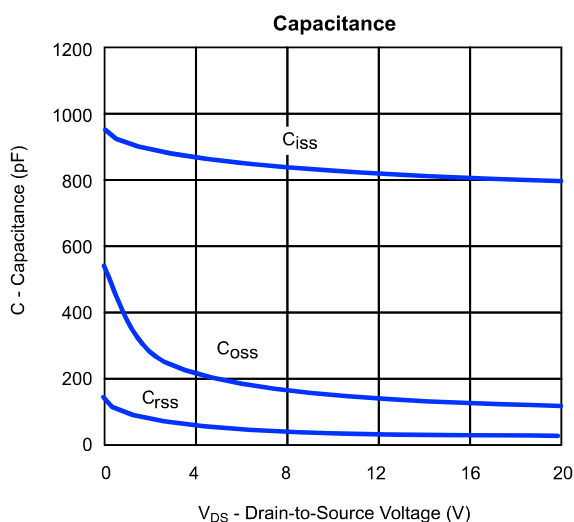
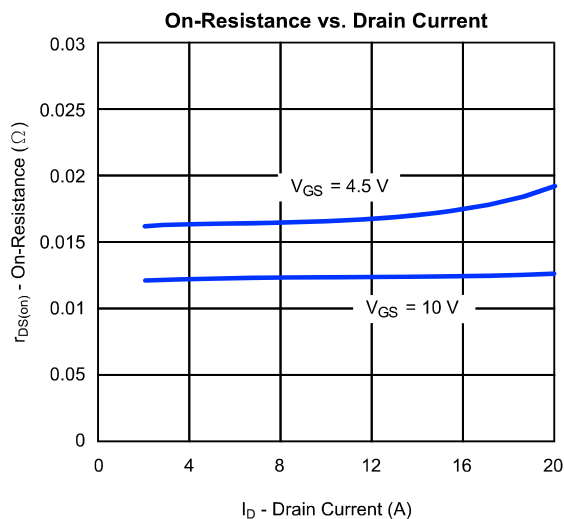
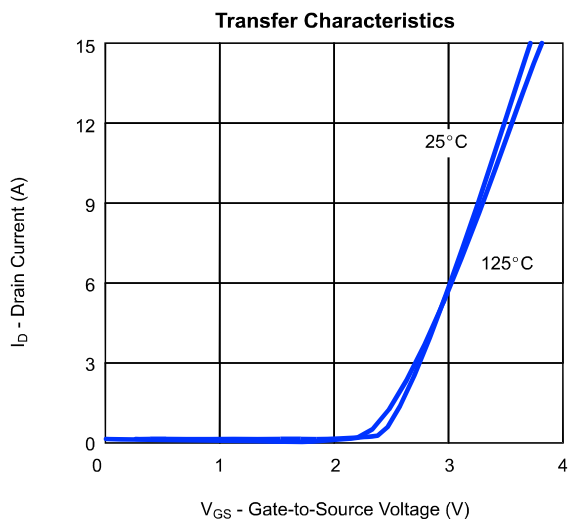
Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	11.6	A
	$T_A=70^\circ\text{C}$		9.2	
Pulsed Drain Current		I_{DM}	46.4	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.08	W
	$T_A=70^\circ\text{C}$		1.33	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	$T \leq 10 \text{ sec}$	35
			Steady State	60

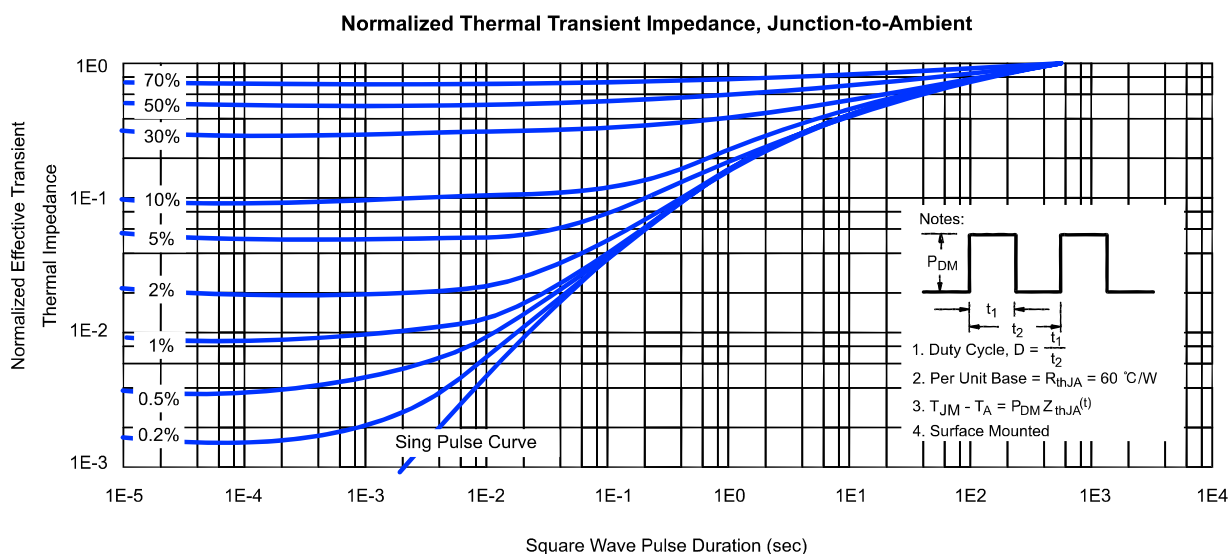
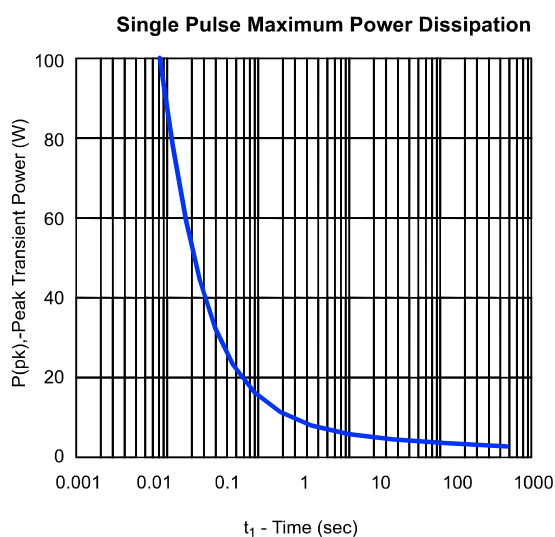
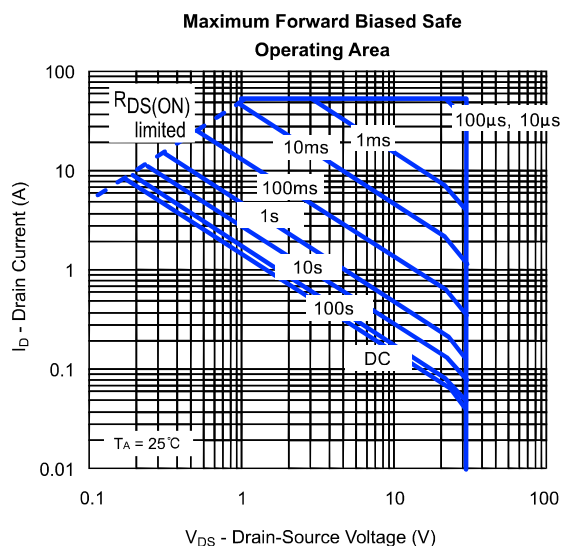
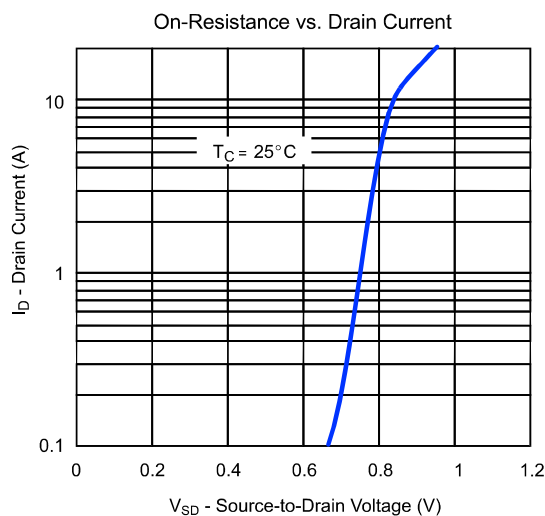
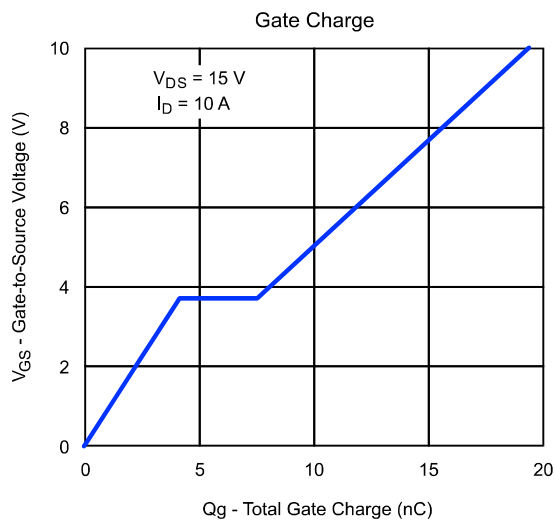
*The device mounted on 1in^2 FR4 board with 2 oz copper

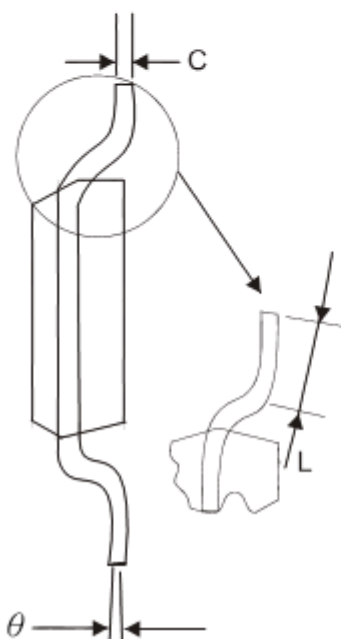
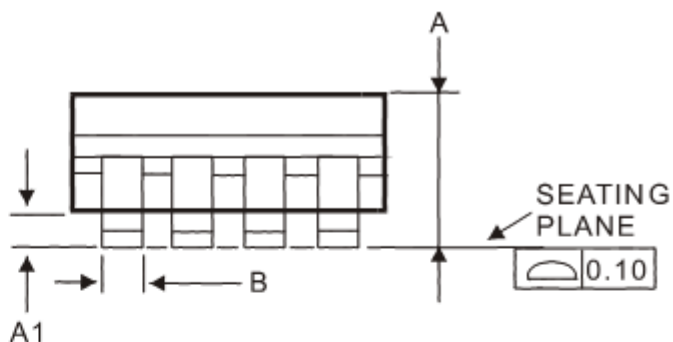
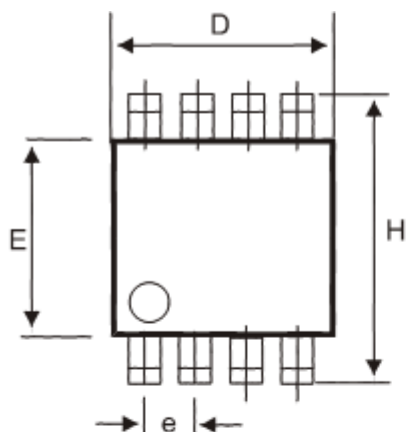
**N-Channel 30-V (D-S) MOSFET****Electrical Characteristics** (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.0	1.4	3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
		V _{DS} =30V, V _{GS} =0V (T _J =55°C)			5	
I _{D(ON)}	On-State Drain Current ^a	V _{DS} =5V, V _{GS} =10V	20			A
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =10A		12	18	mΩ
		V _{GS} =4.5V, I _D =8A		17	20	
G _{FS}	Forward Transconductance ^a	V _{DS} =15V, I _D =10A		17		S
V _{SD}	Diode Forward Voltage	I _S =2.3A, V _{GS} =0V		0.7	1.1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =10A		11	15	nC
Q _{gt}	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =10A		20	26	
Q _{gs}	Gate-Source Charge			5		
Q _{gd}	Gate-Drain Charge			4.9		
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		700	800	pF
C _{oss}	Output Capacitance			120		
C _{rss}	Reverse Transfer Capacitance			35		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.9		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =25V, R _L =25Ω I _D =1A, V _{GEN} =10V R _G =6Ω		14	17	ns
t _r	Turn-On Rise Time			12	15	
t _{d(off)}	Turn-Off Delay Time			43	55	
t _f	Turn-On Fall Time			4	6	

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

**N-Channel 30-V (D-S) MOSFET****Typical Characteristics (T_J =25°C Noted)**

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**SOP-8 Package Outline**

DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.